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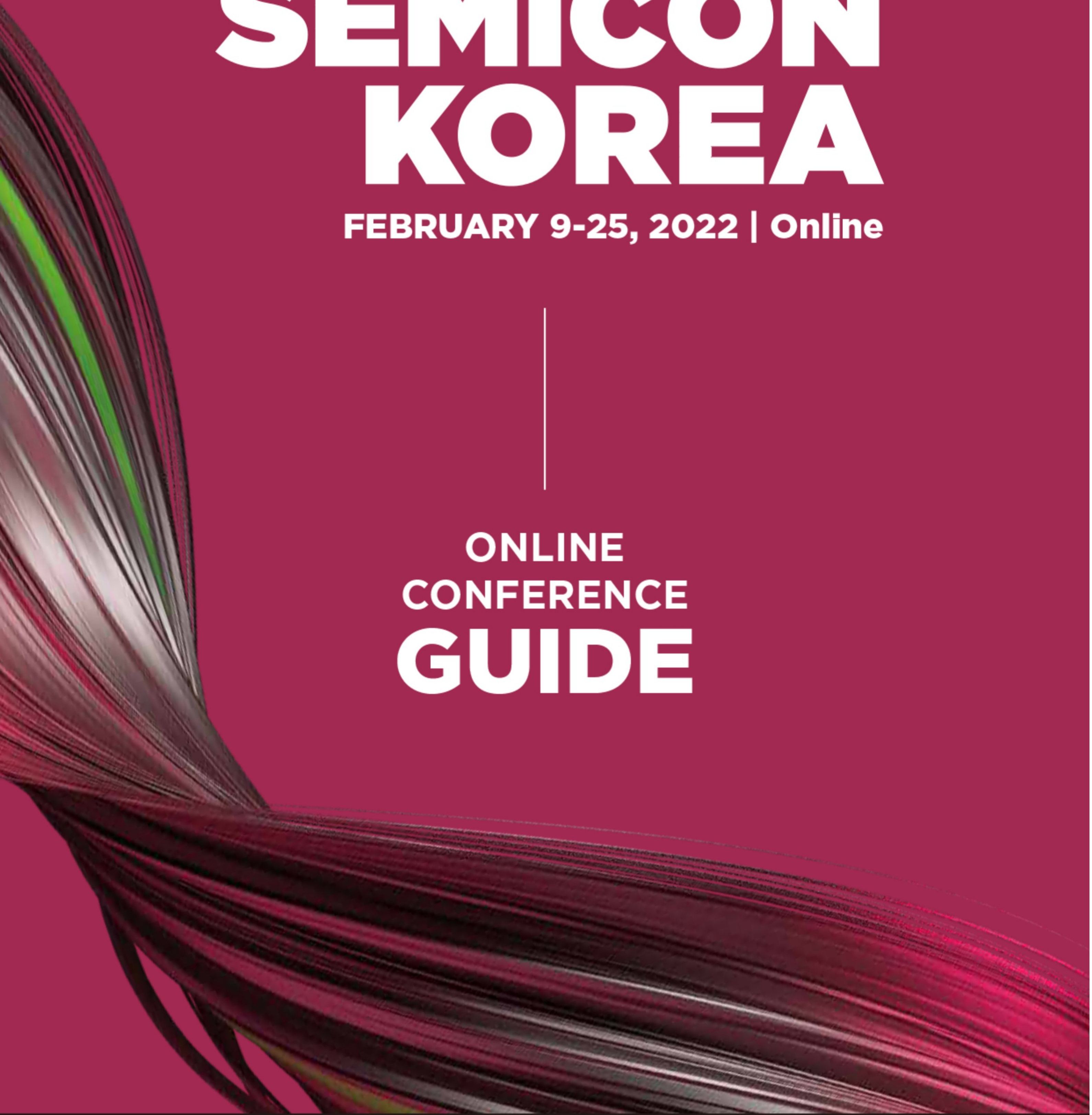
SEMICON® KOREA

FEBRUARY 9-25, 2022 | Online

ONLINE CONFERENCE GUIDE



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Keynote Speech Live	
STS SEMI Technology Symposium	S1. Advanced Lithography S2. Advanced Materials & Process Technology S3. Device Technology S4. Plasma Science and Etching Technology S5. CMP & Cleaning Technology S6. Electropackage System and Interconnect Product
Forum	AI Summit
	Design Automation Forum
	Market Trends Forum
	MEMS & Sensors Summit
	MI Forum
	Smart Manufacturing Forum
	Sustainable Manufacturing Forum
	Test Forum
Workforce Development	Meet the Experts!
DEI (Diversity, Equity, Inclusion)	Women-in-Technology

SEE MORE

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KEYNOTE SPEECH

Wednesday, February 9, 2022

KEYNOTE SPEECH #1

10:00am - 10:30am

Driving Silicon Innovations in a Data-driven Era (KR / 30 Min)

Hyoung-Sub Kim
Head of R&D

SAMSUNG

KEYNOTE SPEECH #2

10:30am - 11:00am

Innovation through Collaboration (EN / 30 Min)

Peter Wennink
CEO

ASML

Thursday, February 10, 2022

KEYNOTE SPEECH #3

10:00am - 10:30am

TBD

Sung Hwan Cho
CEO

HYUNDAI MOBIS

Friday, February 11, 2022

KEYNOTE SPEECH #4

10:00am - 10:30am

Quantum Computers and Future of Computing (EN / 30 Min)

Jungsang Kim
CTO

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S1. Advanced Lithography

EUV High Volume Manufacturing and Beyond

Scaling of cutting-edge products requires continuous advancement of lithography technology as well as timely patterning strategy. EUV lithography is one of the most important technologies for competitive high volume manufacturing. It is essential to expand the current capability of EUV lithography and to study alternative solutions for the next generation lithography. Advanced lithography session of the STS 2022 will provide the best opportunity to understand and discuss the trends in advanced lithography technology under the theme of "EUV High Volume Manufacturing and Beyond". Presentations by academics and companies in the semiconductor industry will offer the most up-to-date information and key progresses in the various areas of advanced lithography. Furthermore, innovative challenges will be discussed to overcome the environmental limitations such as Mask 3D effects and EUV stochastics. Topics will include EUV source, DUV source, exposure tools, optics, materials including CAR and MOR, mask, pellicle, OPC, overlay control, and process integration from the perspectives of various sectors and stake holders of EUV lithography technology. Next-generation technologies, such as high NA EUV and nanoimprint, will be covered in the session as well.

The Current Status of Nano-Imprint Lithography and its Future Outlook toward Carbon Neutrality by 2050 (EN / 30 Min)
Nakasugi Tetsuro | Kioxia (Invited)

EUV Lithography for HVM and Key Progress on its Extension to Lower K1 (EN / 20 Min)
Sung-Woo Lee | ASML

A study of the Impact of Line Edge Roughness on Metal Line Resistance Using Virtual Fabrication (EN / 20 Min)
Qingpeng Wang | Coventor, A Lam Research

Measuring and Controlling Stochastic Variability (EN / 30 Min)
Chris Mack | Fractilia, LLC

Impact of EUV Stochastics Awareness Approach by DUV Mandrel Patterning Together with EUV Source Power Scalability (EN / 30 Min)
Hakaru Mizoguchi | Gigaphoton

Mitigating Challenges of Advanced Patterning Through Innovative Material Developments (EN / 20 Min)
Guanyang Lin | Merck

EUV Pellicle Development Status by S&S TECH (EN / 20 Min)
Byounghoon Seung | S&S Tech

The Fundamental Challenges of Low-Dose EUV Patterning (EN / 20 Min)
Seongbo Shim | Samsung Electornics

Challenges of Overlay Control in EUV Lithography (EN / 20 Min)
Joon geun Ha | SK hynix

Challenges and Solutions for Advanced EUV Resist Process Technology Using CAR and MOR (EN / 20 Min)
Seiji Nagahara | Tokyo Electron

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S2. Advanced Materials & Process Technology

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Pathbreaking Materials and Processes for Nanoscale Semiconductor Technology

In this session, the cutting-edge research and development outputs of Advanced Materials and Process Technology will be shared as the key enablers of the future semiconductor devices. Many prominent authors from the academia and industries will talk key recent achievements regarding the functional materials and semiconductor devices not only in the viewpoints of the fundamental but also of the mass production. Especially, both improvement and disruptive approach to overcome the scaling limit will be discussed in the respect of precursor, equipment, and integration innovation. Excellent 10 presentations including 2 outstanding invited talks will be given to cover the major technical issues and their solutions.

New Materials as a Fundamental Enabler of Next-Generation Logic and Memory Devices (EN / 30 Min)
Steven Scheer | imec (Invited)

Thermal Atomic Layer Etching of Metals Using Chlorination and Ligand-Addition Reactions (EN / 30 Min)
Steven George | University of Colorado (Invited)

Material Innovations for 2nm and Beyond Era (EN / 20 Min)
Bala Haran | Applied Materials

Development and Technical Analysis of New Innovative Logic Architectures Using Semiconductor Process Modeling (EN / 20 Min)
Benjamin Vincent | Coventor, Lam Research

New, Innovative Solutions for Heterogeneous Integration (EN / 20 Min)
CheePing Lee | Lam Research

Solving Interconnected Materials Challenges (EN / 20 Min)
Ron Pearlstein | Merck

Next Generation Deposition Technology for Memory and Logic Application (EN / 20 Min)
Kong Soo Lee | Samsung Electronics

Pathfinding Beyond Memory Devices: Materials Aspect (EN / 20 Min)
Seung Wook Ryu | SK hynix

Advanced Plasma Etch and Deposition Technologies for WBG Device Manufacturing for RF and High Voltage Applications (EN / 20 Min)
Dave Thomas | SPTS Technologies - KLA

Latest Insights on MRAM and XPoint Memory Devices (EN / 20 Min)
Jeongdong Choe | TechInsights

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S3. Device Technology

Innovative Approach to Next-generation Device Technology

Demand for higher performance and lower power has driven device scaling over the last several decades. Both evolutionary and revolutionary innovations have enabled progress in semiconductor devices. Evolutionary path has steered transistor technology towards the state of the art such as gate all around transistors and 2D channel material-based devices. On the other hand, revolutionary ideas have driven transistors towards novel applications such as IOT, AI, automotive, healthcare, and so on.

This session will feature five distinguished speakers to review various novel logic and memory device architectures, and their applications in memory, logic, RF and emerging fields.

Ferroelectric Memory (EN / 30 Min)
Jan Van Houdt | imec (Invited)

WBG Devices for a Sustainable Electrical Energy Future (EN / 30 Min)
Mikael Östling | KTH Royal Institute of Technology (Invited)

Can Two-Dimensional Materials Serve for Future Electronics? (EN / 30 Min)
Lain-Jong (Lance) Li | University of Hong Kong (Invited)

The Challenges and Opportunities on Logic Technology for Innovation (EN / 20 Min)
Dong Il Bae | Samsung Electronics

The Fabrication of 1Xnm 1T1C FE-RAM for Ultra-Thin 5nm-thick HZO and its Low Voltage/High Speed Operation (EN / 20 Min)
Jungwook Woo | SK hynix

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S4. Plasma Science and Etching Technology

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Plasma Etch Technology for 3D DRAM & VNAND

AS the number of VNAND layers goes over 200, the design rule of DRAM goes under 16nm, and Logic devices goes under 3nm generation, the difficulty of etching process has increased abruptly in these days. Especially High Aspect Ratio(HAR) Contact and Line/space patterning got to need the ultra-low loading, the ultra-high selectivity and the very high efficient process monitoring metrology of etching process. So far we have explored the new area of etching technology to respond those needs, for example ultra-high ion energy, Atomic Layer Etch(ALE), various puled plasma and new hard mask materials. But the new needs in the near future will be harsher and tighter and so completely new technologies are necessary. At today symposium we invited many specialists at various etching process areas including HAR contact etching for DRAM/VNAND, plasma damage control, New ALE, virtual metrology and plasma measurement, and especially we invited also speakers of the new agendas, MRAM patterning to replace conventional memories and low GWP(Global Warming Potential) gases to commit the environmental regulations. I expect that all speakers give good insight for the future etching technologies so that all participants at this symposium get to understand the process limitation and the solutions to breakthrough that. For the technology evolves the combined and converged effort by all specialists involved in the technology is essential and the today's symposium will contribute to the new evolution of plasma etching technology.

MRAM Patterning Challenges and Solutions (EN / 30 Min)
Frederic Lazzarino | imec (Invited)

Process Plasma Measurement Technology and Materials/Parts/Equipment Reliability Evaluation Method (EN / 30 Min)
Hyo-Chang Lee | Korea Research Institute of Standards and Science (invited)

Cryogenic Etching Processes Applied to Microelectronics (EN / 30 Min)
Rémi DUSSART | Université d'Orléans (invited)

Moving to Net Zero 2050 – The Importance Of Low Carbon Emission (GWP) In Etch Application (EN / 20 Min)
Chris Jones | Edwards Vacuum

Meeting the Challenges of Next Generation NAND Flash Technology Nodes Through Etch and Deposition Co-optimization (EN / 20 Min)
Meihua Shen | Lam Research

Reducing Plasma Etch Emissions through Molecular Design (EN / 20 Min)
James Nehlsen | Merck

TBD (EN / 20 Min)
Chan Min Lee | Samsung Electronics

Virtual Metrology Combined with Chamber Simulation (EN / 20 Min)
Sangheon Song | SK hynix

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S5. CMP & Cleaning Technology

CMP & Surface Cleaning for Emerging Technology

The fundamental assumptions of scaling according to the Moores law have become increasingly a factor in designing and manufacturing cutting edge semic onductors. As the devices are reaching their physical limits, there still remains many technical challenges to overcome in future. Logic device requires further reduction in power consumption and enhanced speed. DRAM memory needs to shrink to the extreme limits, and 3D NAND structure yet needs to be stacked up higher.

To achieve these, CMP process needs to reduce variation more than now, defect size and micro scratch caused by CMP should be further reduced to below 20 nm. Also, CMP must overcome extreme step height to achieve planarity while at the same time productivity should be secured.

Cleaning process has already gone beyond the concept of just removing normal defects or by-products. The 3D-stucture has become more complex than ever and it requires extremely advanced technology to achieve finely tuned 3D patterns. The limits against the laws of nature in extreme high aspect ratio need constant challenge. Corrosion control, damaged layer control, drying, bulk material removal with very high selective chemical as well as environmental factors must also be carefully considered.

In this session, prominent experts in CMP and Cleaning processes have been invited to discuss the current state and future of some of the challenges in CMP and Cleaning. Reduction of defects caused by CMP to extremely low levels and development of the ultimate drying technology to overcome surface tension are just some of them. A total of 11 topics are presented by world-leading experts from each field.

[CMP Session] Shallow Trench Isolation Chemical Mechanical Planarization: Slurry Chemistry, Cleaning Chemistry, and Mechanisms (EN / 30 Min)

Jihoon Seo | Clarkson University (invited)

[CMP Session] Soft Nanocomposite Electroadhesives for Micro/Nano Particle Manipulation and its Application in Dry Wafer Cleaning (EN / 30 Min)

Sanha Kim | KAIST (invited)

[CMP Session] Formulation Improvement for Polysilicon Post-CMP Clean (EN / 20 Min)

Ping Tzeng | Dupont

[CMP Session] SEMI Standards for Chemical Mechanical Planarization (CMP) Pads and Conditioning Disks (EN / 20 Min)

Alex Tregub | Intel

[CMP Session] Integrated Approach to CMP (EN / 20 Min)

Robert Vacassy | Merck

[CMP Session] Prediction of Chemical Mechanical Planarization(CMP) Profile via Deep Learning Algorithm (EN / 20 Min)

Seung Jun Lee | Samsung Electronics

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S5. CMP & Cleaning Technology

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[Cleaning Session] Modeling and Characterizing the Performance of Fluid Mixing Components in Single-Wafer Wet Processing Equipment for Nanoscale Semiconductor Device Fabrication (EN / 20 Min)

Gary Xing | Ichor

[Cleaning Session] Wafer Backside Issue and Cleaning Challenge (EN / 20 Min)

Won Jun Lee | Samsung Electronics

[Cleaning Session] A Study on Oxide Regrowth and Poly-Silicon Attack of Phosphoric Acid Used in Nitride Strip Process for 3D NAND Device (EN / 20 Min)

Eunseok Oh | SK hynix

[Cleaning Session] A Study of Pattern Leaning Behavior Dependence on Process Conditions of Batch Type Dryer (EN / 20 Min)

Daesung Kim | SK hynix

[Cleaning Session] History of Particle Removal Technology in Wet Cleaning (EN / 20 Min)

Shogo Mizota | TEL

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S6. Electropackage System and Interconnect Product

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Packaging Growth through Technology Diversification

Semiconductor is one of the most important innovations in 20th century. The pandemic caused by Covid 19 has leaded to emerging new lifestyle such as “Contactless” economy. This significant mainstream has accelerated the evolution of our semiconductor society beyond our expectation. As a result, most of package communities has been exposed to shorter development cycles to meet the demand. Herein, S6 in SEMICON Korea is going to hold the following seminars which can help package engineers to expose this environment and make ready for the advancement.

Heterogeneous IC Integration is projected to be a key driver for the next era of Moore’s law. Heterogeneous IC Integration consists of three main topics, Polylithic IC Integration, 2.5D& 3D Integration, and Hybrid Packaging. The second is Fan-out Wafer Level Package which consists of High I/O Density, Higher Productivity, and Higher-degree Heterogeneous Integration Capability. We are going to introduce two presentations related to Wafer Level Integration. In addition, we are going to present two recent developments of electronic materials which play a major role of driving the continuous improvement of semiconductor and package technologies.

2.5D and 3D Polylithic ICs Using Dense Electrical, Photonic, and Monolithic Cooling Technologies for the Next Phase of Moore’s Law (EN / 30 Min)
Muhannad S. Bakir | Georgia Institute of Technology (invited)

Fan-Out Wafer Level Packaging (EN / 30 Min)
Hyoung Joon Kim | Qualcomm (invited)

Advanced Insulating Material for Next-Generation Package (EN / 20 Min)
Yoshio Nishimura | Ajinomoto

Hybrid Packaging Technologies for 5G and Beyond (EN / 20 Min)
JiHun Lee | Amkor Technology Korea

Welco Solder Paste for Fine Pitch RF SiP & Memory Flip Chip Applications (EN / 20 Min)
Lim Thiam Chye | Heraeus

Chiplet PKG Solutions: 2.5D, 3D and Beyond (EN / 20 Min)
Onecheol Bae | Samsung Electronics

WLP Technology Trend in Memory Device
Minsuk Suh | SK hynix

Plasma Etch and Deposition Processes Enabling Hybrid Bonding and Heterogenous Integration
Dave Thomas | SPTS Technologies, KLA

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AI Summit

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AI Hardware

AI & Machine learning is not a concept anymore and it is adopted in design, manufacturing, and automation in semiconductor industry. Also, AI is one of the key factors accompanying the silicon growth with various applications-from daily life gadgets to industrial systems. AI has an infinite potential to expand not only the role of semiconductors but also the market size at the same time. In AI summit, you can meet global expertise from chip makers, fabless and listen to their technology roadmap of AI chip/ business model.

What's Next in AI Hardware: IBM's Partner Ecosystem (EN / 30 Min)
Mukesh Khare | IBM Research (invited)

SAPEON: High-Efficient AI Accelerator for High-Quality AI Services (KR / 30 Min)
Soojung Ryu | SK Telecom (invited)

Accelerating PPACt Scaling with AI, Custom Sensors and Metrology (EN / 30 Min)
Upendra Ummethala | Applied Materials

Scalable Machine Intelligence Systems (EN / 30 Min)
Chris Tunsley | Graphcore

Semiconductor Architecture for Extreme Scale AI (EN / 30 Min)
Andy Hock | Cerebras Systems

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Design Automation Forum

AI Machine Learning

HPC and the big data era brings the new wave in EDA area as well as other industry. Existing algorithm is not sufficient to solve the technical challenge which is more complicated than ever so AI/ML is raising as a novel solution. In this forum, you can learn how the EDA industry is adopting the AI/ML technologies and improving the quality and productivity from global leading EDA professionals.

Journey to the Arm Cloud (EN / 30 Min)
Mark Galbraith | ARM

Improving Productivity and Quality of Results with Machine Learning for EDA (EN / 30 Min)
Frank Schirrmeister | Cadence Design Systems

The Exciting New Super-Cycle in Semiconductors (EN / 30 Min)
Ravi Subramanian | Siemens EDA

Addressing SoC Design Challenges in the Era of SysMoore: From Architecture to Silicon Lifecycle Management (EN / 30 Min)
Shankar Krishnamoorthy | Synopsys

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Market Trends Forum

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What You Can Learn

- Understand the global economy and semiconductor market outlook from various perspectives
- Forecast of the semiconductor industry moves after COVID-19 pandemic
- Automotive chip shortage
- China market

Who Should Attend

- Senior Professionals in Marketing
- Sales
- Procurement
- Business Development
- Consulting and Product Planning
- Finance

Global Memory Outlook - Heterogeneous Computing (KR / 30 Min)
Peter Lee | Citi Group

Supply and Demand Perspective for 2022 and 2023, and Factors Impacting Growth of Chinese Semiconductor Market (EN / 30 Min)
Handel Jones | IBS

Shortage of Chips for Cars: The New Normal? (EN / 30 Min)
Jeremie Bouchaud | IHS Markit

Global Economy (KR / 30 Min)
James Huh | Samsung Securities

Semiconductor Equipment and Materials Outlook (KR / 30 Min)
Sanjay Melhotra | SEMI

2022 Semiconductor Materials Forecast and Challenges (EN / 30 Min)
Dan Tracy | TECHCET

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Smart City Solution by Smart Sensors

Have you ever imagined a future that allows you to access the air quality system of your city with a just one click? Now it is possible, and smart city with more astonishing solution is born with smart sensors all over the world. Smart city solution needs the integration of various sensor systems, and for this, collaboration is the key to success. Find the opportunities for collaboration and meet new business models in here!

KC Digital Drive Air Quality Sensor Program
- Deploying Low Cost Air Quality Sensors as a Citizen Scientist/Community Engagement Project (EN / 20 Min)
Jim Starcev | KC Digital Drive

Smart City Solution in Korea (KR / 20 Min)
Seo Kim | LG CNS

Smart Infrastructure – Technology Trends That Are Changing Traffic & Mobility (EN / 20 Min)
Paul Jacobson | McKinsey & Company

Improving Health and Safety with the Fifth Digital Sense (EN / 20 Min)
Debra Deininger | N5 Sensors

Etch and Deposition Processing of Highly Doped AlScN for PiezoMEMS & RF Filter Applications (EN / 20 Min)
Alex Wood | SPTS Technologies

MEMS Market: Smooth Road Ahead, But...? (EN / 20 Min)
Dimitrios DAMIANOS | Yole Developpement

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MI (Metrology and Inspection) Forum

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Beyond MI - II

Metrology Challenges and Solutions for Next Generation EUV Masks and Patterning Materials (EN / 30 Min)
Patrick Naulleau | Lawrence Berkeley National Laboratory (invited)

Changes in the Role of MI in the Semiconductor Industry and Technological Development Trends (KR / 30 Min)
Younghoon Sohn | Samsung Electronics (invited)

Is High Resolution The Only Solution for One Digit Era? (KR / 30 Min)
Byoung-Ho Lee | SK hynix (invited)

Attosecond Quantum Technologies for Advanced Semiconductor and Materials Metrologies (EN / 30 Min)
Margaret Murnane | University of Colorado (invited)

New Playbook for Process Control Based on Big Data and AI (EN / 20 Min)
Oded Dassa | Applied Materials

In-line 3D Probe Metrology for the Next Generation of Semiconductors (EN / 20 Min)
John Cossins | Infinitesima

Advances in Inspection Methodologies for Advanced Packaging (EN / 20 Min)
Aravindh Vangal | KLA

Enhanced Overlay Stability in Imaging-Based Overlay (IBO) Metrology with rAIM™ Target (20 Min)
Nahee Park | KLA

Spectral Interferometry Usage for Advanced Vertical Integrations Manufacturing Process (EN / 20 Min)
Roy Shtainman | NOVA

TBD (EN / 20 Min)
Kevin Heidrich | Onto Innovation

Plasma Dualbeam Workflow Solutions for Semiconductor Metrology (EN / 20 Min)
Mark Najarian | ThermoFisher Scientific

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Smart Manufacturing Forum

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We are in the way towards Industrial 4.0, which requires Smart Manufacturing technologies and applications to achieve our digital transformation goal. In this forum, you can explore up-to-date intelligence trends particularly for hardware & system in semiconductor manufacturing.

[Keynote] AI in Semiconductor Manufacturing and the Way Forward (EN / 30 Min)
Seonwoo Lee | Merck

Challenges Facing Materials Suppliers in the Post COVID Environment (EN / 20 Min)
Michael Corbett| Linx Consulting

Smart factory for the high-quality semiconductor materials manufacturing (KR / 20 Min)
Louis Lim | Miracom Inc.

How to Build a Sustainable Smart Manufacturing through the Application of Digital Technology in Semiconductor (KR / 20 Min)
Seung-Hyun Choi | Schneider Electric

From Reactive to Predictive: Smart Manufacturing in the Semiconductor Industry - The MADEin4 Initiative (EN / 20 Min)
Olaf Kievit | TNO

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Sustainable Manufacturing Forum

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Sustainability is one of today's hottest topics in the news, and improving sustainability performance is a growing priority for SEMI Member companies. Given its central role in technology innovation, the electronics manufacturing industry has a responsibility to be a leader in sustainability and companies are actively developing their strategies to address the many challenges.

The Sustainable Manufacturing Forum will focus on the industry's efforts, highlighting topics such as greenhouse gas emissions reduction, increased renewable energy utilization, and enhanced equipment energy and water efficiency.

[Keynote] Sustainability for All (KR / 30 Min)
Claire Seo | Samsung Electronics

Advanced Wet Scrubber – Essential for VOC Control and Process Stability (EN / 20 Min)
Tino Tanneberger | DAS Environmental Expert

Paving the Way to a More Sustainable Future by Purpose-Driven Global Innovation (EN / 20 Min)
Rick Hemond | DuPont

Focusing on Fab Metrics to Achieve Collaborative and Sustainable Operations Between the SubFab and Cleanroom (EN / 20 Min)
Erik Collart | Edwards Vacuum

TBD (EN / 20 Min)
John McLaughlin | KLA

Introduction to SEMI Sustainability Initiative (EN / 20 Min)
James Amano | SEMI

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Test Forum

Last year was one of the most turbulent years for the semiconductor industry.

With the rapid growth of the Metaverse, AI, Big Data, AR, VR, and 5G markets, the semiconductor was reorganized, and also following the entire semiconductor shortage including automotive semiconductors.

In the meantime, advances in semiconductor test technology, which makes it possible to test even all 300 million transistors per square millimeter fabricated by the most advanced 3nm process, has become the last essential element to supply high-quality semiconductors to the rapidly growing market in the most timely and economical manner.

Test Forum will be a good opportunity to share and learn the secrets of the most necessary cutting-edge semiconductor test technology in the present and future.

Addressing Test Cell Technical and Complexity Challenges to Accelerate Time to Yield (EN / 20 Min)
Ian Lawee | Cohu

The Future of Digital Test: PAM4 (EN / 20 Min)
David Raschko | Formfactor

Modernizing the Lab: Using a Software-Centric Approach in a Hardware-Centric World (EN / 20 Min)
Ritu Favre | NI

Automotive Semiconductor Market Growth for Functional Safety (EN / 20 Min) (EN / 20 Min)
Sungsoo Chung | QRT

Semiconductor Test in the GAA Era (EN / 20 Min)
Rick Burns | Teradyne

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Meet the Experts!

Workforce development is more important than ever since semiconductor industry is getting bigger and bigger. Industry is focusing on catching young talents' eyes and encouraging them to be involved in the industry as an engineer. As part of this effort, Meet the Experts! - the Mentoring Seminar is prepared for university students. You can meet the engineers from diverse backgrounds and hear what you really want to know by participating here.

Keynote (KR / 30 Min)
Hyeon Deok Lee | Wonik IPS

Customer Engineer (KR / 20 Min)
Jaegwang Shin | Applied Materials

CS Engineer (KR / 20 Min)
Kyung-Uk Lee | ASML

Technical Support Engineer (KR / 20 Min)
Yeonghan Yun | KLA

Process Engineer (KR / 20 Min)
Jaeho Lee | Lam Research

Process Engineer (KR / 20 Min)
Sangjong Park | PSK

Design (KR / 20 Min)
Yagob Kim | SEMES

Software (KR / 20 Min)
Byoung Min Im | Tokyo Electron

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Women-in-Technology

As diversity is regarded as one of the most significant competitiveness, women in the workforce become an important issue of global economy. According to the Report on the Status of Women in Science, Engineering and Technology in Korea, women account for about 20% of the R&D workforce and various efforts have been made to give more opportunities for women and to expand their roles. Women in Technology will bring together leaders who drive the changes to discuss how we can improve the diversity in the industry.

[KEYNOTE] Women in Semiconductor: Designing Your Future (EN & Sub-title: KR / 20 Min)
Deirdre Hanford | Synopsys

Female in Sales (KR / 20 Min)
Bok-Hee Lee | DuPont Korea

Dive into the Possibilities (KR / 20 Min)
Nicole Shin | Lam Research

Building My Career in Engineering (KR / 20 Min)
Sarah Eunkyung Kim | Seoul National University of Science and Technology

Slowly, but Surely (KR / 20 Min)
Chanjin Kim | Siemens EDA

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